

	L #	Hits	Search Text	DBs
1	L1	2862	((indicat\$3 flag tag bit field mode) near10 ((utiliz\$3 us\$3 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near10 prediction))	USPAT; US-PGPUB
2	L4	838	prediction near10 (effective ineffective reliab\$5 low confidence hard difficult acccura\$3 inaccura\$3) and 1	USPAT; US-PGPUB
3	L5	102	4 and (branch and prediction).ab,ti.	USPAT; US-PGPUB

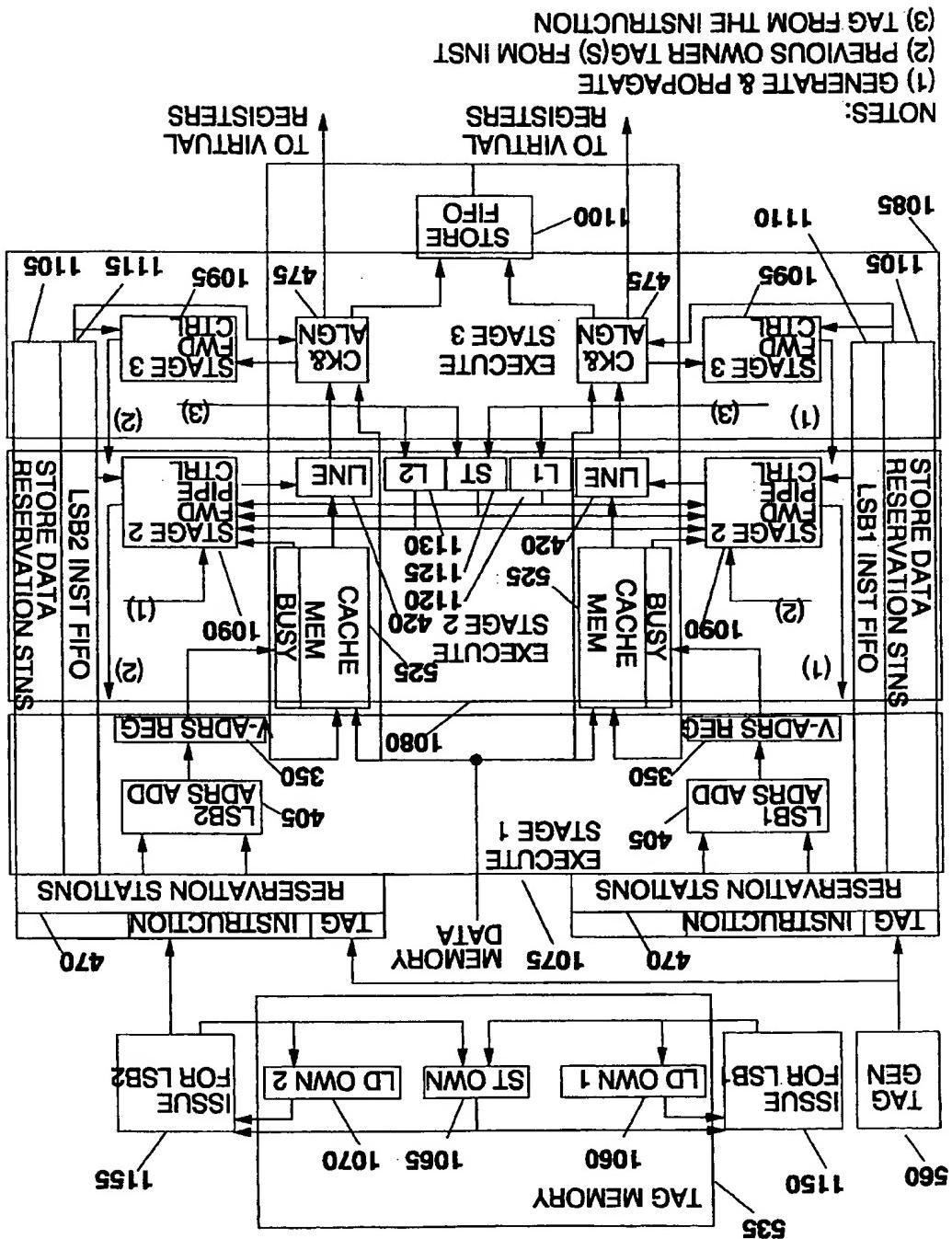
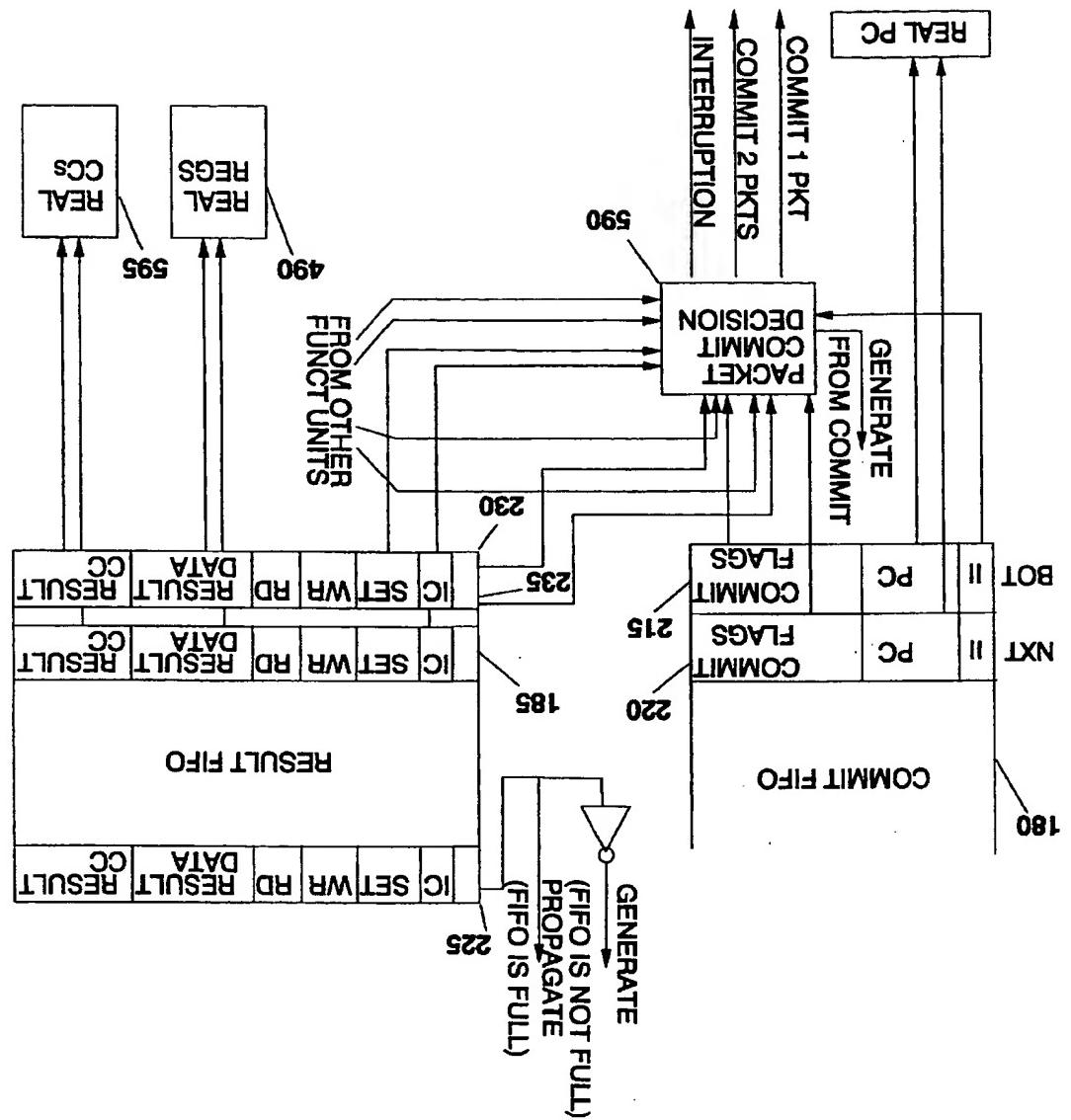


Figure 27e. Invention,  
Dynamic Scheduling Embodiment,  
Tagged Memory Tagging

	Document ID	U	Title	Current OR
1	US 20040 03083 8 A1	<input type="checkbox"/>	Instruction cache way prediction for jump targets	711/137
2	US 20030 08427 1 A1	<input checked="" type="checkbox"/>	Speculative execution for java hardware accelerator	712/209
3	US 20030 06591 2 A1	<input checked="" type="checkbox"/>	Removing redundant information in hybrid branch prediction	712/239
4	US 20030 04123 0 A1	<input checked="" type="checkbox"/>	METHOD AND SYSTEM FOR BRANCH TARGET PREDICTION USING PATH INFORMATION	712/238
5	US 20020 19446 4 A1	<input checked="" type="checkbox"/>	Speculative branch target address cache with selective override by secondary predictor based on branch instruction type	712/239
6	US 20020 19446 3 A1	<input checked="" type="checkbox"/>	Speculative hybrid branch direction predictor	712/239
7	US 20020 19446 2 A1	<input checked="" type="checkbox"/>	Apparatus and method for selecting one of multiple target addresses stored in a speculative branch target address cache per instruction cache line	712/238
8	US 20020 19446 1 A1	<input checked="" type="checkbox"/>	Speculative branch target address cache	712/238
9	US 20020 18883 3 A1	<input checked="" type="checkbox"/>	Dual call/return stack branch prediction system	712/236
10	US 20020 13823 6 A1	<input checked="" type="checkbox"/>	Processor having execution result prediction function for instruction	702/186
11	US 20020 07833 2 A1	<input checked="" type="checkbox"/>	Conflict free parallel read access to a bank interleaved branch predictor in a processor	712/240
12	US 20020 07330 1 A1	<input checked="" type="checkbox"/>	Hardware for use with compiler generated branch information	712/235
13	US 20020 02933 3 A1	<input checked="" type="checkbox"/>	Methods and apparatus for branch prediction using hybrid history with index sharing	712/239
14	US 20010 04746 7 A1	<input checked="" type="checkbox"/>	METHOD AND APPARATUS FOR BRANCH PREDICTION USING FIRST AND SECOND LEVEL BRANCH PREDICTION TABLES	712/228
15	US 20010 03744 6 A1	<input checked="" type="checkbox"/>	Processor and branch prediction method	712/239
16	US 20010 03230 9 A1	<input checked="" type="checkbox"/>	Static branch prediction mechanism for conditional branch instructions	712/239
17	US 20010 02026 7 A1	<input checked="" type="checkbox"/>	Pipeline processing apparatus with improved efficiency of branch prediction, and method therefor	712/239



Dynamic Scheduling Embodiment  
Real Registers and CCs,  
Figure 27f, Invention,

	Docum ent ID	U	Title	Current OR
18	US 20010 01690 3 A1	<input checked="" type="checkbox"/>	Software branch prediction filtering for a microprocessor	712/239
19	US 20010 01134 6 A1	<input checked="" type="checkbox"/>	Branch prediction method, arithmetic and logic unit, and information processing apparatus	712/239
20	US 66786 38 B2	<input checked="" type="checkbox"/>	Processor having execution result prediction function for instruction	702/186
21	US 66623 60 B1	<input checked="" type="checkbox"/>	Method and system for software control of hardware branch prediction mechanism in a data processor	717/131
22	US 66622 95 B2	<input checked="" type="checkbox"/>	Method and system dynamically presenting the branch target address in conditional branch instruction	712/234
23	US 66402 98 B1	<input checked="" type="checkbox"/>	Branch prediction apparatus	712/239
24	US 66011 61 B2	<input checked="" type="checkbox"/>	Method and system for branch target prediction using path information	712/238
25	US 65981 52 B1	<input checked="" type="checkbox"/>	Increasing the overall prediction accuracy for multi-cycle branch prediction and apparatus by enabling quick recovery	712/228
26	US 65713 31 B2	<input checked="" type="checkbox"/>	Static branch prediction mechanism for conditional branch instructions	712/239
27	US 65534 88 B2	<input checked="" type="checkbox"/>	Method and apparatus for branch prediction using first and second level branch prediction tables	712/239
28	US 65105 11 B2	<input checked="" type="checkbox"/>	Methods and apparatus for branch prediction using hybrid history with index sharing	712/240
29	US 65021 88 B1	<input checked="" type="checkbox"/>	Dynamic classification of conditional branches in global history branch prediction	712/234
30	US 64991 01 B1	<input checked="" type="checkbox"/>	Static branch prediction mechanism for conditional branch instructions	712/239
31	US 64272 06 B1	<input checked="" type="checkbox"/>	Optimized branch predictions for strongly predicted compiler branches	712/239
32	US 64250 75 B1	<input checked="" type="checkbox"/>	Branch prediction device with two levels of branch prediction cache	712/239
33	US 63857 20 B1	<input checked="" type="checkbox"/>	Branch prediction method and processor using origin information, relative position information and history information	712/240
34	US 63743 51 B1	<input checked="" type="checkbox"/>	Software branch prediction filtering for a microprocessor	712/239
35	US 63413 48 B1	<input checked="" type="checkbox"/>	Software branch prediction filtering for a microprocessor	712/239
36	US 63321 90 B1	<input checked="" type="checkbox"/>	Branch prediction method using a prediction table indexed by fetch-block address	712/240
37	US 62826 29 B1	<input checked="" type="checkbox"/>	Pipelined processor for performing parallel instruction recording and register assigning	712/23
38	US 62791 07 B1	<input checked="" type="checkbox"/>	Branch selectors associated with byte ranges within an instruction cache for rapidly identifying branch predictions	712/239
39	US 62726 24 B1	<input checked="" type="checkbox"/>	Method and apparatus for predicting multiple conditional branches	712/239

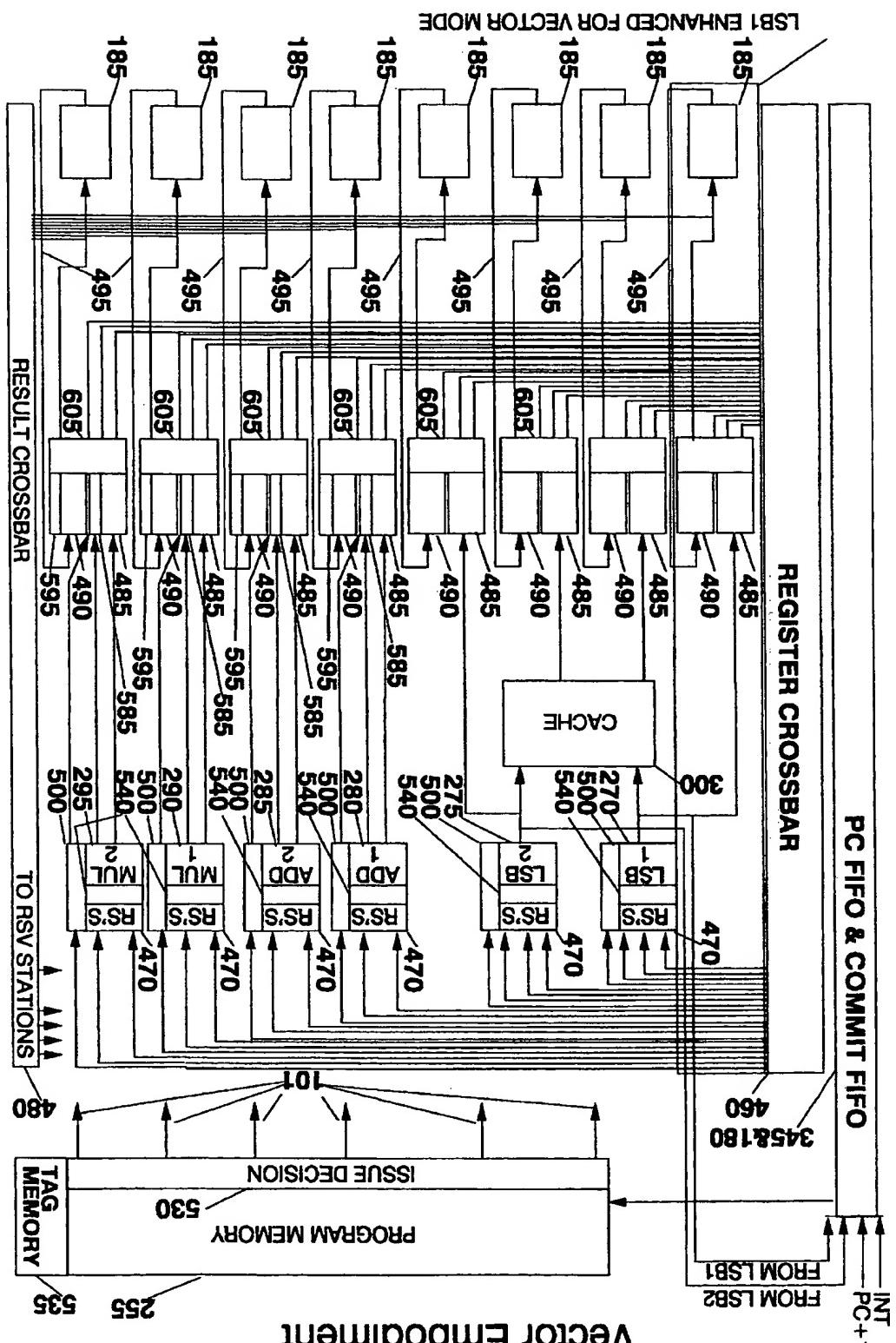
**Figure 28. Invention, Vector Embedment**

5,471,593

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Nov. 28, 1995

U.S. Patent



	Document ID	U	Title	Current OR
40	US 62726 23 B1	<input checked="" type="checkbox"/>	Methods and apparatus for branch prediction using hybrid history with index sharing	712/239
41	US 62694 36 B1	<input checked="" type="checkbox"/>	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
42	US 62533 16 B1	<input checked="" type="checkbox"/>	Three state branch history using one bit in a branch prediction mechanism	712/239
43	US 62471 23 B1	<input checked="" type="checkbox"/>	Branch prediction mechanism employing branch selectors to select a branch prediction	712/239
44	US 62471 22 B1	<input checked="" type="checkbox"/>	Method and apparatus for performing branch prediction combining static and dynamic branch predictors	712/239
45	US 62336 79 B1	<input checked="" type="checkbox"/>	Method and system for branch prediction	712/240
46	US 61784 98 B1	<input checked="" type="checkbox"/>	Storing predicted branch target address in different storage according to importance hint in branch prediction instruction	712/239
47	US 61700 53 B1	<input checked="" type="checkbox"/>	Microprocessor with circuits, systems and methods for responding to branch instructions based on history of prediction accuracy	712/240
48	US 61579 99 A	<input checked="" type="checkbox"/>	Data processing system having a synchronizing link stack and method thereof	712/243
49	US 61417 48 A	<input checked="" type="checkbox"/>	Branch selectors associated with byte ranges within an instruction cache for rapidly identifying branch predictions	712/239
50	US 61087 74 A	<input checked="" type="checkbox"/>	Branch prediction with added selector bits to increase branch prediction capacity and flexibility with minimal added bits	712/240
51	US 60818 87 A	<input checked="" type="checkbox"/>	System for passing an index value with each prediction in forward direction to enable truth predictor to associate truth value with particular branch instruction	712/239
52	US 60676 16 A	<input checked="" type="checkbox"/>	Branch prediction device with two levels of branch prediction cache	712/239
53	US 60556 29 A	<input checked="" type="checkbox"/>	Predicting for all branch instructions in a bunch based on history register updated once for all of any taken branches in a bunch	712/239
54	US 60527 76 A	<input checked="" type="checkbox"/>	Branch operation system where instructions are queued until preparations is ascertained to be completed and branch distance is considered as an execution condition	712/233
55	US 60292 28 A	<input checked="" type="checkbox"/>	Data prefetching of a load target buffer for post-branch instructions based on past prediction accuracy's of branch predictions	711/137
56	US 60165 45 A	<input checked="" type="checkbox"/>	Reduced size storage apparatus for storing cache-line-related data in a high frequency microprocessor	712/238
57	US 60147 34 A	<input checked="" type="checkbox"/>	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
58	US 59957 49 A	<input checked="" type="checkbox"/>	Branch prediction mechanism employing branch selectors to select a branch prediction	712/239
59	US 59833 35 A	<input checked="" type="checkbox"/>	Computer system having organization for multiple condition code setting and for testing instruction out-of-order	712/23
60	US 59789 06 A	<input checked="" type="checkbox"/>	Branch selectors associated with byte ranges within an instruction cache for rapidly identifying branch predictions	712/239
61	US 59745 42 A	<input checked="" type="checkbox"/>	Branch prediction unit which approximates a larger number of branch predictions using a smaller number of branch predictions and an alternate target indication	712/239
62	US 59616 38 A	<input checked="" type="checkbox"/>	Branch prediction mechanism employing branch selectors to select a branch prediction	712/239

CYC	FETCH	INST	ISSUE	SELECT	EXECUTE	INPUTS	STAGE 1	R48	C48 MODE
1	103	102	101	100	PC = 104 FROM LOOP 104 @ 100	3	?	ON	
2	104(1)	103	102	101	PC = 104 FROM LOOP	3	?	ON	
3	104(2)	104(1)	103	102	PC = 104 FROM R50	3	?	ON	
4	104(3)	104(2)	104(1)	103	PC = 104 FROM R50	3	?	ON	
5	104(4)	104(3)	104(2)	104(1)	PC = 104 FROM R50	2	POS	ON	
6	104(5)	104(4)	104(3)	104(2)	PC = 104 FROM R50	1	POS	ON	
7	104(6)	104(5)	104(4)	104(3)	PC = 104 FROM R50	0	ZERO OFF		
8	105	104(6)	104(5)	104(4)	PC = 104 + 1 (R48=0)	0	ZERO OFF		
9	106	105	104(6)	104(5)	PC = 105 + 1	0	ZERO OFF		
10	107	106	105	104(6)	PC = 106 + 1	0	ZERO OFF		
11	108	107	106	105	PC = 107 + 1	0	ZERO OFF		

ADDRS	LSB1	INST	LSB2	INSTR	ANY	ANY	TOTAL OF 10 LOCATIONS
100	LOOP 104	STORE R1,R2,A1,IR					
101	ANY	STORE R1,R2,A1,IR					
102	ANY	STORE R1,R2,A1,IR					
103	ANY	STORE R1,R2,A1,IR					
104	DEC/SET	STORE R1,R2,A1,IR					
105	ANY	STORE R1,R2,A1,IR					
106	ANY	STORE R1,R2,A1,IR					
107	ANY	ANY					

R48 = 6-3      R49 = 104      R50 = 104

### One-Packet Vector Loop Example

Figure 29. Invention,

	Document ID	U	Title	Current OR
63	US 59548 16 A	<input checked="" type="checkbox"/>	Branch selector prediction	712/239
64	US 59499 95 A	<input checked="" type="checkbox"/>	Programmable branch prediction system and method for inserting prediction operation which is independent of execution of program code	712/239
65	US 59352 41 A	<input checked="" type="checkbox"/>	Multiple global pattern history tables for branch prediction in a microprocessor	712/240
66	US 59338 60 A	<input checked="" type="checkbox"/>	Multiprobe instruction cache with instruction-based probe hint generation and training whereby the cache bank or way to be accessed next is predicted	711/213
67	US 59283 58 A	<input checked="" type="checkbox"/>	Information processing apparatus which accurately predicts whether a branch is taken for a conditional branch instruction, using small-scale hardware	712/239
68	US 59013 07 A	<input checked="" type="checkbox"/>	Processor having a selectively configurable branch prediction unit that can access a branch prediction utilizing bits derived from a plurality of sources	712/240
69	US 58965 29 A	<input checked="" type="checkbox"/>	Branch prediction based on correlation between sets of bunches of branch instructions	712/239
70	US 58813 08 A	<input checked="" type="checkbox"/>	Computer organization for multiple and out-of-order execution of condition code testing and setting instructions out-of-order	712/23
71	US 58812 78 A	<input checked="" type="checkbox"/>	Return address prediction system which adjusts the contents of return stack storage to enable continued prediction after a mispredicted branch	712/242
72	US 58753 25 A	<input checked="" type="checkbox"/>	Processor having reduced branch history table size through global branch history compression and method of branch prediction utilizing compressed global branch history	712/240
73	US 58647 07 A	<input checked="" type="checkbox"/>	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
74	US 58646 97 A	<input checked="" type="checkbox"/>	Microprocessor using combined actual and speculative branch history prediction	712/240
75	US 58482 69 A	<input checked="" type="checkbox"/>	Branch predicting mechanism for enhancing accuracy in branch prediction by reference to data	712/239
76	US 58357 54 A	<input checked="" type="checkbox"/>	Branch prediction system for superscalar processor	712/239
77	US 58357 45 A	<input checked="" type="checkbox"/>	Hardware instruction scheduler for short execution unit latencies	712/215
78	US 58288 74 A	<input checked="" type="checkbox"/>	Past-history filtered branch prediction	712/240
79	US 58225 75 A	<input checked="" type="checkbox"/>	Branch prediction storage for storing branch prediction information such that a corresponding tag may be routed with the branch instruction	712/239
80	US 57940 28 A	<input checked="" type="checkbox"/>	Shared branch prediction structure	712/240
81	US 57404 15 A	<input checked="" type="checkbox"/>	Instruction supplying apparatus with a branch target buffer having the contents so updated as to enhance branch prediction accuracy	712/238
82	US 57297 07 A	<input checked="" type="checkbox"/>	Instruction prefetch circuit and cache device with branch detection	712/207
83	US 56873 60 A	<input checked="" type="checkbox"/>	Branch predictor using multiple prediction heuristics and a heuristic identifier in the branch instruction	712/240
84	US 56491 37 A	<input checked="" type="checkbox"/>	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/207
85	US 56301 57 A	<input checked="" type="checkbox"/>	Computer organization for multiple and out-of-order execution of condition code testing and setting instructions	712/23

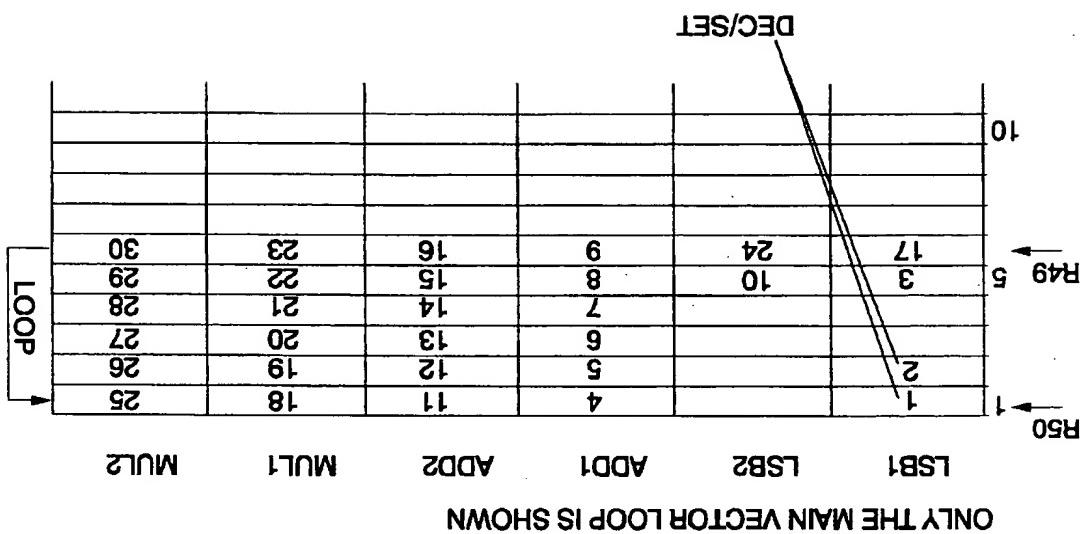


Figure 30. Invention,  
LFK24 Main Loop Mapping,  
Vector Embodiment

	Docum ent ID	U	Title	Current OR
86	US 56196 62 A	<input checked="" type="checkbox"/>	Memory reference tagging	712/216
87	US 55817 19 A	<input checked="" type="checkbox"/>	Multiple block line prediction	712/207
88	US 55772 17 A	<input checked="" type="checkbox"/>	Method and apparatus for a branch target buffer with shared branch pattern tables for associated branch predictions	712/200
89	US 55641 18 A	<input checked="" type="checkbox"/>	Past-history filtered branch prediction	712/240
90	US 55532 55 A	<input checked="" type="checkbox"/>	Data processor with programmable levels of speculative instruction fetching and method of operation	712/235
91	US 55532 53 A	<input checked="" type="checkbox"/>	Correlation-based branch prediction in digital computers	712/240
92	US 55198 41 A	<input checked="" type="checkbox"/>	Multi instruction register mapper	711/202
93	US 55155 18 A	<input checked="" type="checkbox"/>	Two-level branch prediction cache	712/239
94	US 55111 75 A	<input checked="" type="checkbox"/>	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/216
95	US 53815 33 A	<input checked="" type="checkbox"/>	Dynamic flow instruction cache memory organized around trace segments independent of virtual address line	712/215
96	US 53275 47 A	<input checked="" type="checkbox"/>	Two-level branch prediction cache	711/137
97	US 53136 34 A	<input checked="" type="checkbox"/>	Computer system branch prediction of subroutine returns	712/240
98	US 52261 30 A	<input checked="" type="checkbox"/>	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/238
99	US 51631 40 A	<input checked="" type="checkbox"/>	Two-level branch prediction cache	711/140
100	US 51426 34 A	<input checked="" type="checkbox"/>	Branch prediction	712/240
101	US 50937 78 A	<input checked="" type="checkbox"/>	Integrated single structure branch prediction cache	712/240
102	US 44307 06 A	<input type="checkbox"/>	Branch prediction apparatus and method for a data processing system	712/237

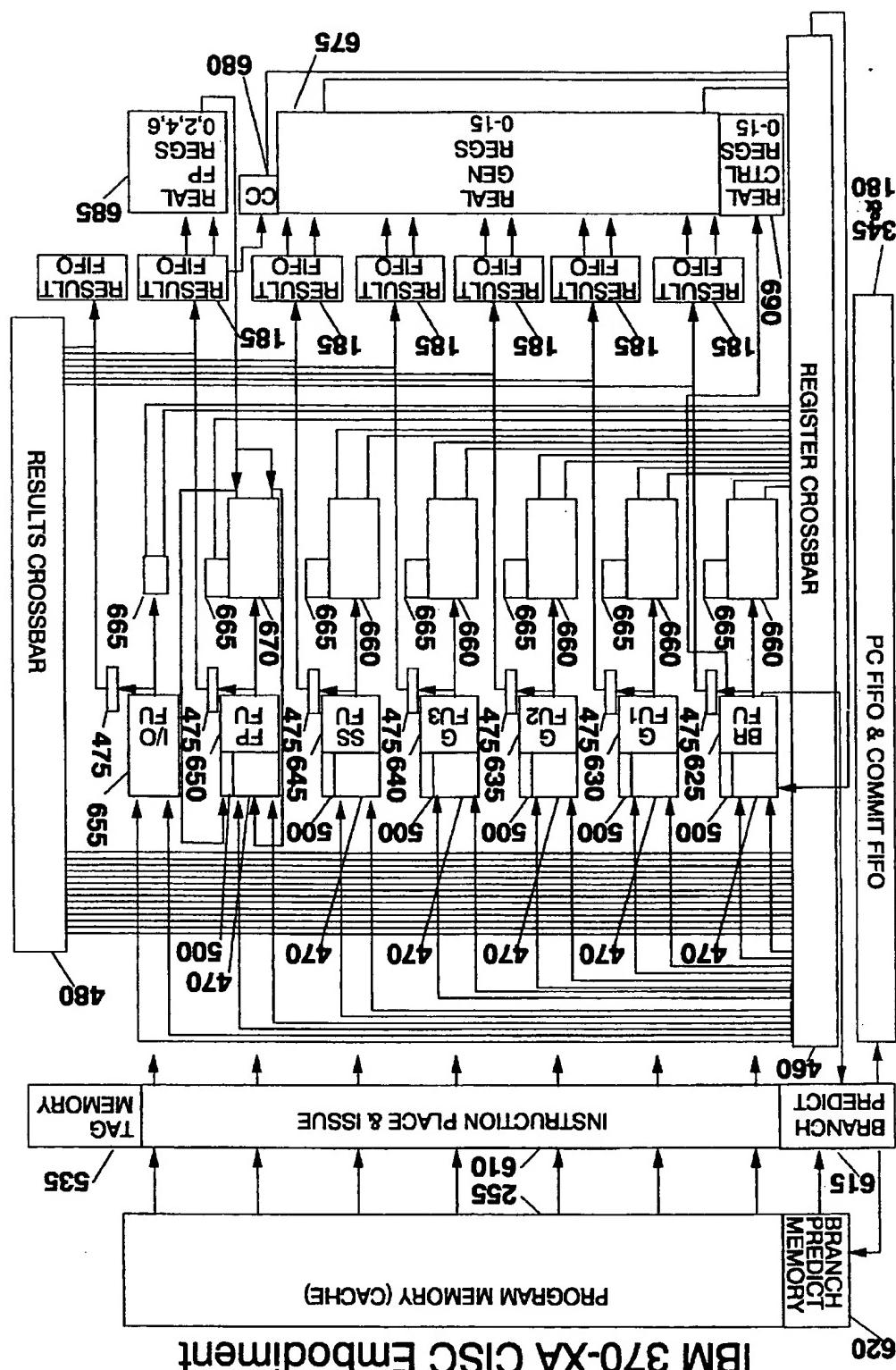


Figure 31a. Invention,